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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,735	01/14/2004	Paul J. Garnett	5681-78000	4872

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EXAMINER
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LEVI, DAMEON E

ART UNIT	PAPER NUMBER
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2841

DATE MAILED: 05/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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<b>Office Action Summary</b>	<b>Application No.</b> 10/757,735	<b>Applicant(s)</b> GARNETT ET AL.	
	<b>Examiner</b> Dameon E. Levi	<b>Art Unit</b> 2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 14 January 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-21 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 January 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

**Claims 1-3, and 7-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Danovitch et al US Patent 6819566.**

**Regarding claim 1**, Danovitch et al discloses an assembly comprising:

an electrically conductive shielding portion(for example, see element 16, Figs 1-5) mountable adjacent the electronic component (for example, see element 11, Figs 1-5) at least partially to surround the electronic component; and at least one resiliently biased electrically conductive connection member(for example, see element 21, Fig 4) in electrical communication with the shielding portion (for example, see element 16, Fig 4) and operable electrically to connect the shielding

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portion to a predetermined voltage by bearing down upon an electrically conductive contact of (for example, see element 18, Fig 4) the circuit board (for example, see element 13, Fig 4).

**Regarding claim 2**, Danovitch et al discloses wherein a surface of the shielding portion defines a cavity (for example, see element 20, Fig 4) for receiving one of the at least one connection members.

**Regarding claim 3**, Danovitch et al discloses comprising a plurality of said connection members and wherein the surface of the shielding portion defines a plurality of cavities each for receiving a respective one of the connection members (for example, see elements 21, 20, 22, 23, Figs 3-5, also see column 5, lines 15-25).

**Regarding claim 7**, Danovitch et al discloses comprising a retainer (for example, see elements 22) for preventing removal of the at least one connecting member from the cavity.

**Regarding claim 8**, Danovitch et al discloses wherein the shielding portion is mounted on the electronic component (for example, see elements 16, 11, Figs 1-5).

**Regarding claim 9**, Danovitch et al discloses comprising a mounting strut (for example, see element 19, Figs 2, 3) for mounting the shielding portion on the circuit board.

**Regarding claim 10**, Danovitch et al discloses comprising a plurality of said connection members arranged to extend along a peripheral edge of said electronic component to form a shielding cage around said component (for example, see elements 22-26, Figs 3-5).

**Regarding claim 11**, Danovitch et al discloses further comprising one or more support

members, each support member being attached to at least two connection members to provide support therefor(for example, see support members on elements 16, Fig 3).

**Regarding claim 12**, Danovitch et al discloses wherein the one or more support members are electrically conductive(for example, see column 2, lines 15-30).

**Regarding claim 13**, Danovitch et al discloses wherein at least one of the electrically conductive shielding portion and said at least one electrically conductive connection member are metal(for example, see column 5, lines 15-30).

**Regarding claim 14**, Danovitch et al discloses an assembly comprising:

an electrically conductive shielding portion (for example, see element 16, Figs 1-5) mounted adjacent the electronic component (for example, see element 11, Figs 1-5) and at least partially surrounding the electronic component; and at least one resiliently biased electrically conductive connection member(for example, see element 21, Figs 1-5) in electrical communication with the shielding portion and electrically connecting the shielding portion to the predetermined voltage by bearing down upon the electrically conductive contact(for example, see element 18, Figs 1-5).

**Regarding claim 15**, Danovitch et al discloses wherein the electrical contact comprises an electrically conductive surface layer(for example, see element 18, Figs 1-5).

**Regarding claim 16**, Danovitch et al discloses further comprising an opening in the circuit board in which said connection member is received, an interior surface of the opening being coated with an electrically conductive layer forming said electrically conductive contact(for example, see opening in element 13, in which element 18, is received, Figs 2-4).

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**Regarding claim 17**, Danovitch et al discloses comprising a plurality of said connection members, each connection member bearing down upon the electrically conductive contact(for example, see element 21,18, Fig 4).

**Regarding claim 18**, Danovitch et al discloses the circuit board having a plurality of said electrically conductive contacts(for example, see element 18, Fig 4), the EM shielding assembly comprising a plurality of said connection members(for example, see element 21, Fig 4), each connection member bearing down upon a respective one of the electrically conductive contacts.

**Regarding claim 19**, Danovitch et al discloses an assembly comprising:  
electrically conductive shielding means(for example, see element 16, Figs 1-5)  
mountable adjacent the electronic component at least partially to surround the electronic component(for example, see element 11, Figs 1-5); and  
resiliently biased electrically conductive connection means(for example, see element 21, Figs 1-5) in electrical communication with the shielding means and operable electrically to connect the shielding means to a predetermined voltage by bearing down upon an electrically conductive contact(for example, see element 18, Figs 1-5) of the circuit board.

**Regarding claim 20**, Danovitch et al discloses an assembly comprising:  
electrically conductive shielding means(for example, see element 16, Figs 1-5)  
mounted adjacent the electronic component and at least partially surrounding the electronic component(for example, see element 11, Figs 1-5);and

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resiliently biased electrically conductive connection means(for example, see element 21, Figs 1-5) in electrical communication with the electrically conductive shielding means and electrically connecting the electrically conductive shielding means to the predetermined voltage by bearing down upon the electrically conductive contact means(for example, see element 18, Figs 1-5).

**Regarding claim 21**, the methods disclosed therein are deemed as being inherent in the assembly and operation of the claimed invention since Danovitch et al teaches the structural elements of the claims.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

**Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over**

**Danovitch et al US Patent 6819566 in view of Gonsalves et al US Patent 6212074.**

**Regarding claim 4**, Danovitch et al discloses the instant claimed invention except the shielding portion having a first plurality of cooling members extending away therefrom, each cooling member accommodating a respective one of said cavities.

Gonsalves et al discloses an assembly with a shielding portion having a first plurality of cooling members extending away therefrom, each cooling member

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accommodating a respective one of said cavities(for example, see cooling fins on elements 30, cavities therein accommodating elements 60-1, Figs 1-3).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included cooling members extending away therefrom, as well as, to include cavities therein in the manner as taught by Gonsalves et al in the assembly as taught by Danovitch et al as such cooling members are known in the art as cooling fins used for increased heat dissipation from the electronic device, as well as, to use the cavities to insert a contact device for securing the assembly as a whole.

**Regarding claim 5**, Danovitch et al discloses the instant claimed invention except the shielding portion having a second plurality of cooling members extending away therefrom.

Gonsalves et al discloses an assembly with a shielding portion having a second plurality of cooling members extending away therefrom(for example, see cooling fins on elements 30, Figs 1-3).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included cooling members extending away therefrom, in the manner as taught by Gonsalves et al in the assembly as taught by Danovitch et al as such cooling members are known in the art as heat sink cooling fins used for increased heat dissipation from the electronic device.

**Regarding claim 6**, Danovitch et al discloses the instant claimed invention except wherein the first plurality of cooling members are arranged around a periphery of the electronic component.



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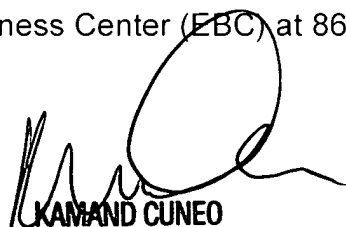
Gonsalves et al discloses an assembly wherein the first plurality of cooling members are arranged around a periphery of the electronic component (for example, see cooling fins on elements 30, Figs 1-3).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have arranged the cooling members in the manner as taught by Gonsalves et al in the assembly as taught by Danovitch et al as such an arrangement would provide increased heat dissipation from the electronic device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dameon E. Levi whose telephone number is (571) 272-2105. The examiner can normally be reached on Mon.-Fri. (9:00 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
**KAMAND CUNEO**  
**SUPERVISORY PATENT EXAMINER**  
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